Figure 1-3

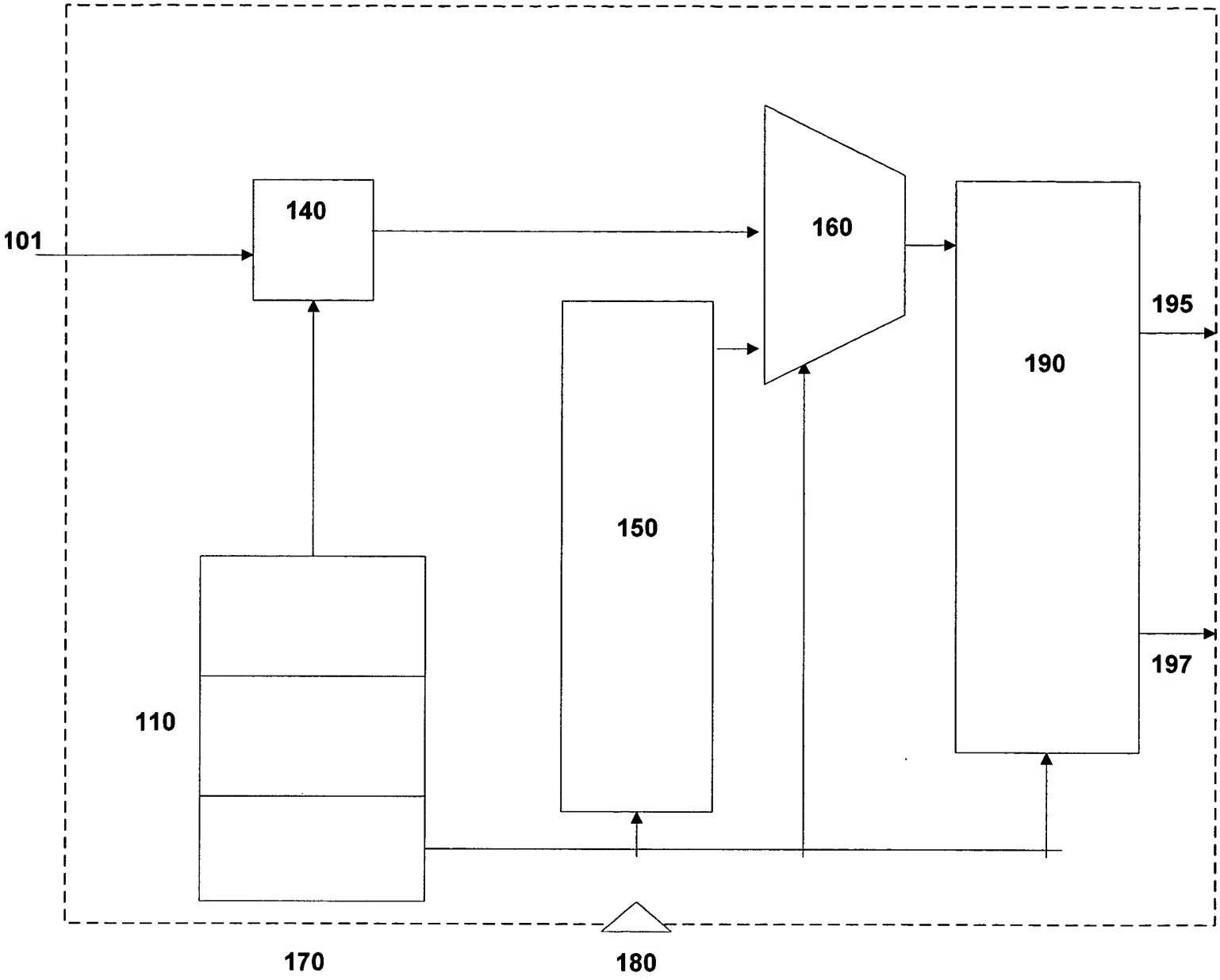


Figure 2-3

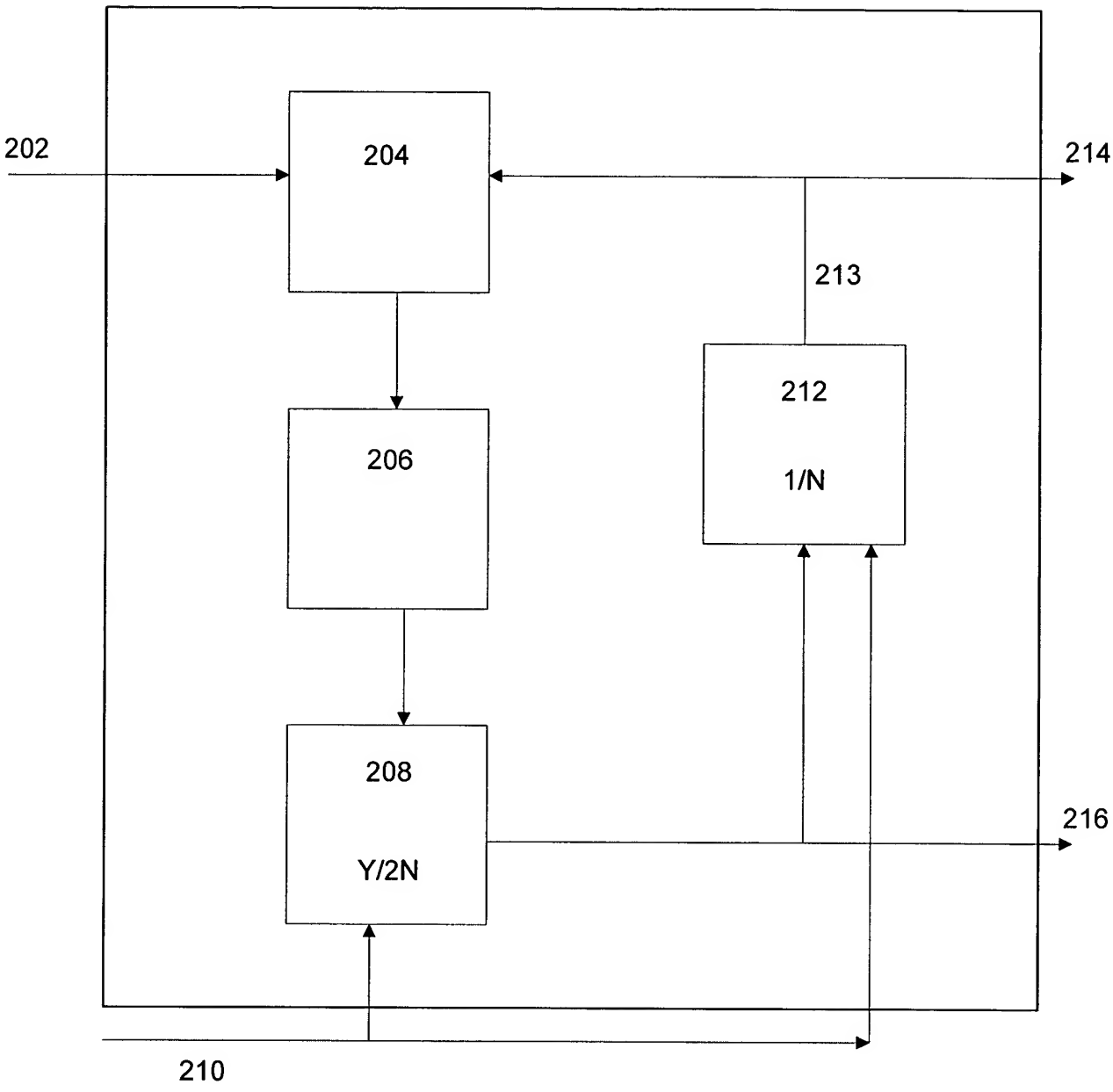
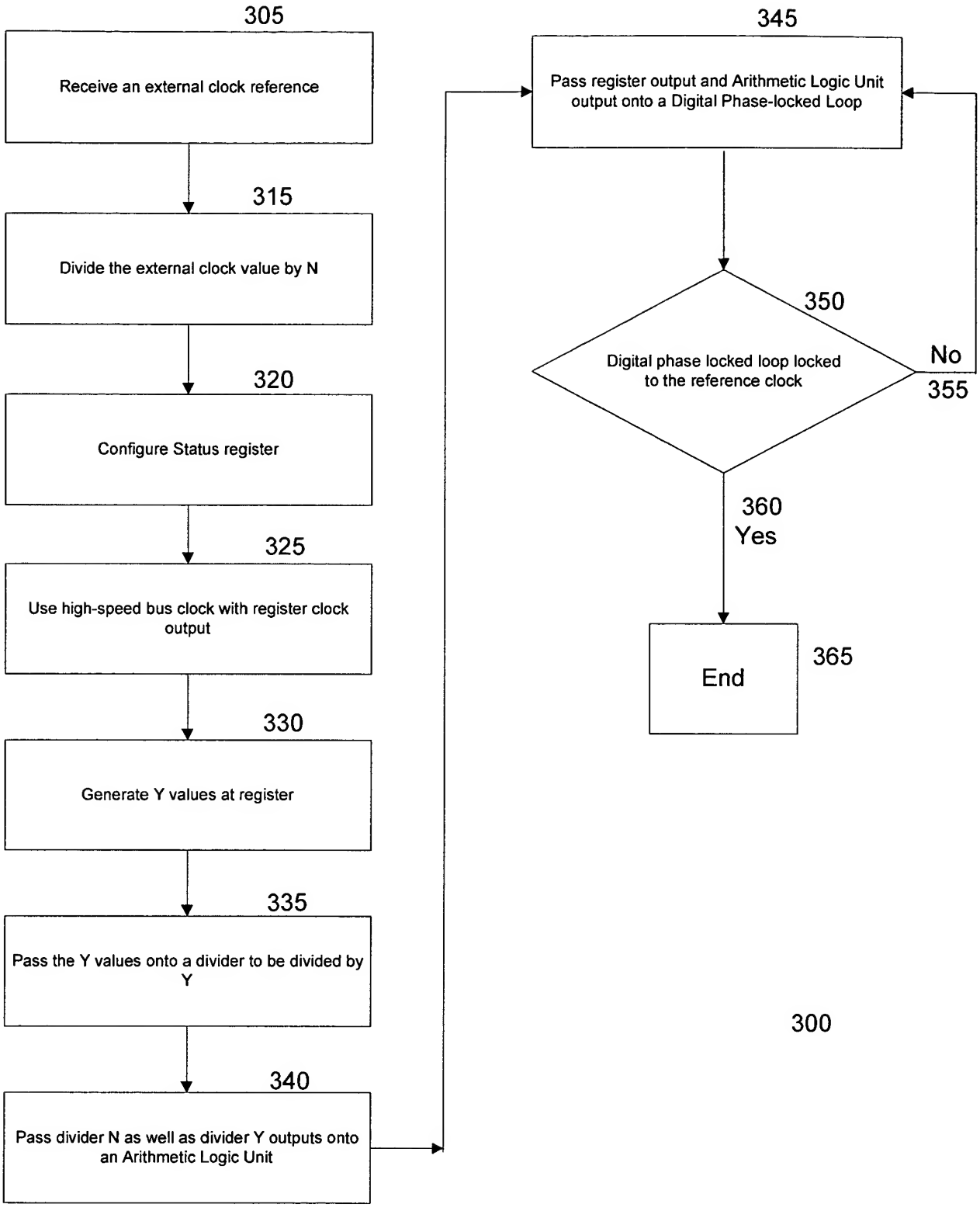


Figure 3-3


305
Receive an external clock reference
315
Divide the external clock value by N
320
Configure Status register
325
Use high-speed bus clock with register clock output
330
Generate Y values at register
335
Pass the Y values onto a divider to be divided by Y
340
Pass divider N as well as divider Y outputs onto an Arithmetic Logic Unit
345
Pass register output and Arithmetic Logic Unit output onto a Digital Phase-locked Loop
350
Digital phase locked loop locked to the reference clock
No
355
360
Yes
End
365
300